NOTICE OF REVISION (NOR)

THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED.

1. DATE (YYMMDD) 96-03-13

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME *(First, Middle Initial, Last)*

b. ADDRESS *(Street, City, State, Zip Code)*
Defense ElectronicsSupply Center
1507 Wilmington Pike
Dayton, OH 45444-5270

5. CAGE CODE 67268

6. NOR NO. 5962-R058-96

7. CAGE CODE 67268

8. DOCUMENT NO. **5962-91545**

9. TITLE OF DOCUMENT
MICROCIRCUIT, MEMORY,DIGITAL,CMOS,UV ERASEABLE, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

10. REVISION LETTER

a. CURRENT C

b. NEW D

11. ECP NO. NONE

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
All

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "D".
Revisions description column; add "Changes in accordance with NOR 5962-R058-96".
Revisions date column; add "96-03-13".
Rev status above sheet numbers 1, 6, 10, and 20, change from "C" to "D".
Revision level block; change from "C" to "D".

Sheet 6: Table I, parameter Output Capacitance change limit from 8 pF to 12 pF max.
Revision level block; change from "C" to "D".

Sheet 10: Paragraph 4.2.1b delete entirely and replace with the following: "Devices shall be burned-in containing a pattern that assures all inputs and I/Os are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized)."
Revision level block; change from "C" to "D".

Sheet 20: On table IIA, line 2 Static burn-in; in the blocks under the column headings for Device class M and Device class Q add footnote 8/. Go to bottom of footnotes, and add footnote 8/ to read "Either static or dynamic burn-in may be performed.
Revision level block; change from "C" to "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT
DESC-ELDS

c. TYPED NAME *(First, Middle Initial, Last)*
Michael A. Frye

d. TITLE
Chief, Microelectronics Team

e. SIGNATURE
Michael A. Frye

f. DATE SIGNED (YYMMDD) 96-03-13

15a. ACTIVITY ACCOMPLISHING REVISION
DESC-ELDS

b. REVISION COMPLETED *(Signature)*
Kenneth S. Rice

c. DATE SIGNED (YYMMDD) 96-03-13

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added low power version, device type 03, with an access time of 35 ns for CAGE number IFN41. Editorial changes throughout.	92-10-29	M. A. Frye
B	Changes in accordance with NOR 5962-R182-93	93-06-03	M. A. Frye
C	Added four devices (04-07). Editorial changes throughout.	95-05-19	M. A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	C	C	C	C	C	C	C	C											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael Frye

DRAWING APPROVAL DATE
91-07-25

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS UV ERASABLE PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-91545**

SHEET 1 OF 22

DESC FORM 193
JUL 94

5962-E145-95

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	91545	01	M	Q	X
Federal stock class designator	RHA designator (See 1.2.1)		Device type (See 1.2.2)	Device class designator (See 1.2.3)	Case outline (See 1.2.4)	Lead finish (See 1.2.5)
\ Drawing number /						

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Standby Supply Current
01	V2500H	38-input, 24-output and-or-logic array	35 ns	
02	V2500H	38-input, 24-output and-or-logic array	25 ns	
03	V2500L	38-input, 24-output and-or-logic array	35 ns	10 mA
04	V2500B	38-input, 24-output and-or-logic array	15 ns	
05	V2500BL	38-input, 24-output and-or-logic array	20 ns	10 mA
06	V2500BQ	38-input, 24-output and-or-logic array	25 ns	
07	V2500BQL	38-input, 24-output and-or-logic array	30 ns	5 mA

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line 1/
X	CQCC1-N44	44	Square leadless chip carrier 1/
Y	See figure 1	44	J-leaded chip carrier 1/

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 4/
Output voltage range applied	-0.5 V dc to +7.0 V dc 4/
Output sink current	8 mA
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Q, X	See MIL-STD-1835
Case Y	20°C/W
Maximum power dissipation (P_D) 5/	1.2 W
Maximum junction temperature	+175°C
Lead temperature (soldering, 10 seconds maximum)	+300°C
Endurance	25 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.0 V dc minimum
Low level input voltage range (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	6/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to V_{SS}.
4/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
5/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
6/ Values will be added when a qualified source is available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.3 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of gates programmed).

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Verification of erasure or programmed EPLD's. When specified, devices shall be verified as either programmed (see 4.7 herein) to the specified pattern or erased (see 4.6 herein). As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract.

3.6.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.7 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.7.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.8 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.9 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.11 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.12 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitor. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific but shall gurantee the number of program/erase endurance cycles listed in section 1.3 herein. This procedure shall be under document control and shall be made available upon request.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_O = -4.0 mA, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_O = 6.0 mA, V_{IH} = 2.0 V	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		25	µA
		V_{IH} = 2.4 V				10	
Low level input current	I_{IL}	V_{IL} = 0.4 V	1, 2, 3	All		-10	µA
		V_{IL} = GND				-10	
Supply current	I_{CC1}	Outputs open, V_{CC} = 5.5 V, V_{IN} = GND or V_{CC}	1, 2, 3	01-03		180	mA
				04,05		210	
				06,07		85	
Standby supply current	I_{CC2}	V_{CC} = 5.5 V, V_{IN} = GND or V_{CC} Outputs open	1, 2, 3	03,05		10	mA
				07		5	
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V	1, 2, 3	01-03	-30	-90	mA
				04-07	-30	-120	
Input capacitance	C_I 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		8	pF
Output capacitance	C_O 4/ 5/	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)	4	All		8	pF
Functional tests		see 4.4.1c	7,8A,8B	All			
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF, see figures 5 and 6 (circuit A)	9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Input to output disable	t_{ER}		9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = * pF, see figures 5 and 6 (* circuit B or C as applicable)	9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Clock to output	t_{CO}		9, 10, 11	01,03		35	ns
				02,06		25	
				04		15	
				05		20	
				07		30	
Clock period (t_{CF} + t_{SF})	t_P	V_{CC} = 4.5 V, C_L = 5 pF, see figures 5 and 6 (circuit A)	9, 10, 11	01,03	35		ns
				02	25		
				04	17		
				05	24		
				06	28		
				07	30		
Clock pulse width	t_W	V_{CC} = 4.5 V, C_L = * pF, see figures 5 and 6 (* circuit B or C as applicable)	9, 10, 11	01	15		ns
				02	10		
				03	17		
				04	7.5		
				05	11		
				06	14		
				07	15		
Clock to feedback	t_{CF}		9, 10, 11	01	15	20	ns
				02	10	18	
				03	15	20	
				04	5	12	
				05	10	16	
				06	12	18	
				07	13	20	
Setup time 6/ output register	t_{SI1}		9, 10, 11	01	15		ns
				02	10		
				03	22		
				04	5		
				05	10		
				06	15		
				07	19		
Setup time 7/ buried register	t_{SI2}		9, 10, 11	01,02	5		ns
				03	22		
				04	5		
				05	10		
				06	15		
				07	19		
Feedback setup time	t_{SF}		9, 10, 11	01,03	15		ns
				02	7		
				04	5		
				05	8		
				06,07	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Hold time	t_H	V_{CC} = 4.5 V, C_L = * pF, see figures 5 and 6 (* circuit B or C as applicable)	9, 10, 11	01,02, 04	5		ns
				05	10		
				06	12		
				07	13		
Hold time output register	t_{H1}		9, 10, 11	03	15		ns
Hold time buried register	t_{H2}		9, 10, 11	03	5		ns
Maximum clock frequency 4/ 6/	f_{MAX}		9, 10, 11	01,03		28	MHz
				02		40	
				04		66	
				05		45	
				06		36	
				07		33	
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01,03	20		ns
				02	15		
				04	8		
				05	12		
				06	15		
				07	18		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01,03	20		ns
				02	15		
				04	8		
				05	12		
				06	15		
				07	18		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01,03		35	ns
				02		25	
				04		18	
				05		22	
				06		28	
				07		30	
Clock to output, input pin clock	t_{COS}		9, 10, 11	04		10	ns
				05		11	
				06		12	
				07		15	
Clock to feedback, input pin clock	t_{CFS}		9, 10, 11	04	0	5	ns
				05	0	6	
				06	0	7	
				07	0	8	
Input setup time, input pin clock	t_{SIS}		9, 10, 11	04	9		ns
				05	14		
				06	20		
				07	23		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, -55° C ≤ T_C ≤ +125° C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Feedback setup time, input pin clock	t_{SFS}	V_{CC} = 4.5 V, C_L = * pF, see figures 5 and 6 (* circuit B or C as applicable)	9, 10, 11	04	9		ns
				05	14		
				06	20		
				07	23		
Hold time, input pin clock	t_{HS}		9, 10, 11	04	0		ns
				05	0		
				06	0		
				07	0		
Clock width, input pin clock	t_{WS}		9, 10, 11	04	6		ns
				05	7		
				06	8		
				07	9		
Clock period, input pin clock	t_{PS}		9, 10, 11	04	12		ns
				05	14		
				06	16		
				07	18		
Maximum clock frequency input pin clock	f_{MAXS}		9, 10, 11	04		83	MHz
				05		71	
				06		62	
				07		55	
Asynchronous reset/ preset recovery time, input pin clock	t_{ARS}		9, 10, 11	04	12		ns
				05	15		
				06	20		
				07	25		
Feedback to non-registered output	t_{PD2}		9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	
Input to nonregistered feedback	t_{PD3}		9, 10, 11	04		11	ns
				05		15	
				06		18	
				07		20	
Feedback to non-registered feedback	t_{PD4}		9, 10, 11	04		11	ns
				05		15	
				06		18	
				07		20	
Feedback to output enable	t_{EA2}	V_{CC} = 4.5 V, C_L = 5 pF see figures 5 and 6 (circuit A)	9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	
Feedback to output disable	t_{ER2}		9, 10, 11	04		15	ns
				05		20	
				06		25	
				07		30	

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.

TABLE I. Electrical performance characteristics - Continued.

3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to register outputs.
7/ Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinational.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as 3.1.9 through 3.1.13 (preburn-in electrical parameters through interim postburn-in electrical parameters of method 5004) and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.7 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot. The manufacturer as an option may use built-in test circuitry by testing the entire lot to verify programmability and AC performance without programming the user array.

c. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test.

Method A. (Steps 1 through 4 may be performed at wafer level.)

(1) Program at +25°C with a greater than 95 percent pattern (example, diagonal "1's") (see 3.5).

(2) Unbiased bake for 24 hours at +175°C.

(3) Test at T_C = +75°C, including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

(4) Erase.

(5) Program at +25°C with a checkerboard pattern (see 3.5).

(6) Test at T_C = +125°C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

(7) Burn-in (see 4.2.1c).

(8) Perform electrical tests at T_C = +25° C, including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

(9) Perform electrical tests at T_C = +125° C (minimum), including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

(10) Perform electrical tests at T_C = -55° C, including a margin test at Vm = +6 V and loose timing (i.e., t_{AVQV} = 1 µs).

(11) Erase (see 3.5). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100-percent seal tested in accordance with method 5004 of MIL-STD-883.

(12) Verify erasure at +25° C (see 3.5).

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

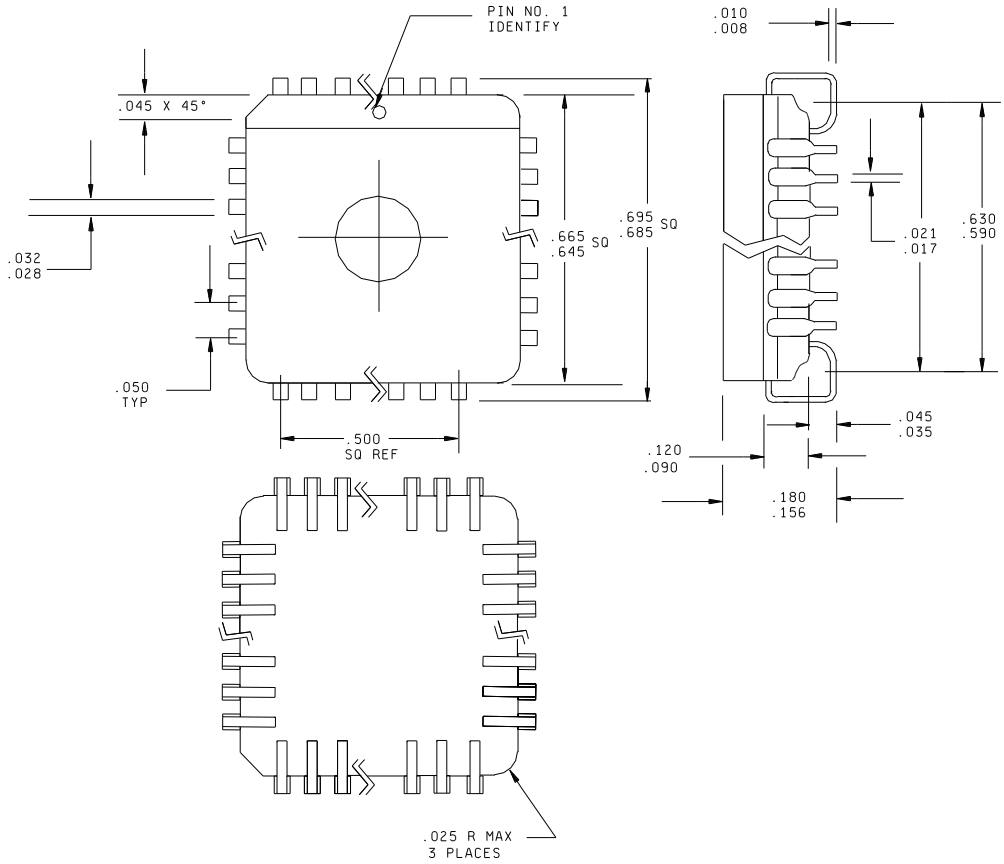
4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M subgroups 7, 8A and 8B tests shall consist of verifying functionality of the device. These tests form a part of the vendors test tape and shall be maintained and available upon request. For device classes Q and V subgroups 7, 8A and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.



Inches	mm	Inches	mm	Inches	mm
.008	0.20	.045	1.14	.590	15.00
.010	0.25	.050	1.27	.630	16.00
.017	0.43	.090	2.29	.645	16.40
.021	0.53	.120	3.05	.665	16.90
.025	0.64	.156	3.96	.685	17.40
.028	0.71	.180	4.57	.695	17.70
.032	0.81	.500	12.70		
.035	0.89				

NOTES:
1. The US goverment preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline.

Device types	All	
Case outlines	Q	X, Y
Terminal number	Terminal symbol	
1	I	I
2	I	I
3	I	I
4	I/O	NC
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	V_{CC}	I/O
11	I/O	V_{CC}
12	I/O	V_{CC}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I	I/O
18	I	I/O
19	I	I
20	I	I
21	I	I
22	I	I
23	I	I
24	I/O	I
25	I/O	I
26	I/O	NC
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	GND	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	GND
34	I/O	GND
35	I/O	I/O
36	I/O	I/O
37	I	I/O
38	I	I/O
39	I	I/O
40	I	I/O
41	---	I
42	---	I
43	---	I
44	---	I

FIGURE 2. Terminal connections.

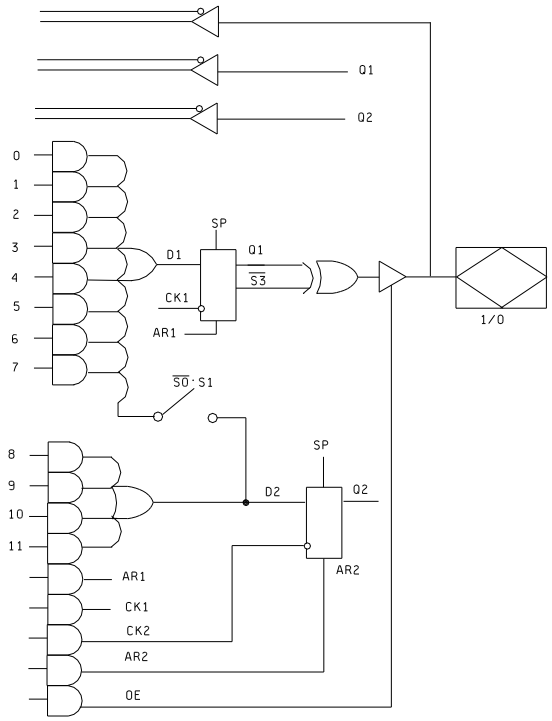
Input pins														Output pins											
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Output pins - continued											
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

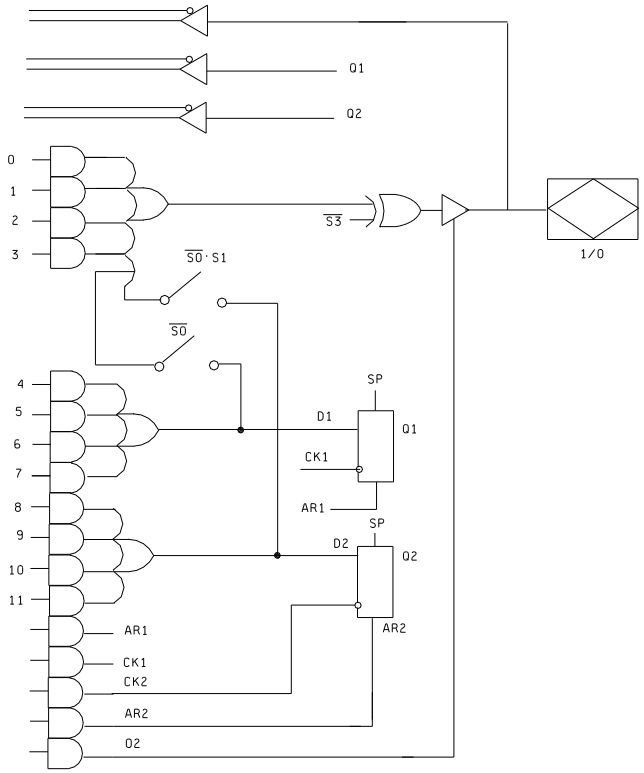
X = Don't care state
Z = Three-state

FIGURE 3. Truth table.

Output logic, registered



Output logic, combinational



NOTE: These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

S2 S1 S0	Terms in D1 S2	Output configuration
0 0 0	8 4	Registered (Q1)
0 1 0	12 4*	Registered (Q1)

* (See note)

S2 S1 S0	Terms in D1 D2	Output configuration
1 0 0	4* 4	Combinatorial (8 terms)
1 0 1	4 4	Combinatorial (4 terms)
1 1 0	4* 4*	Combinatorial (12 terms)

*(See note)

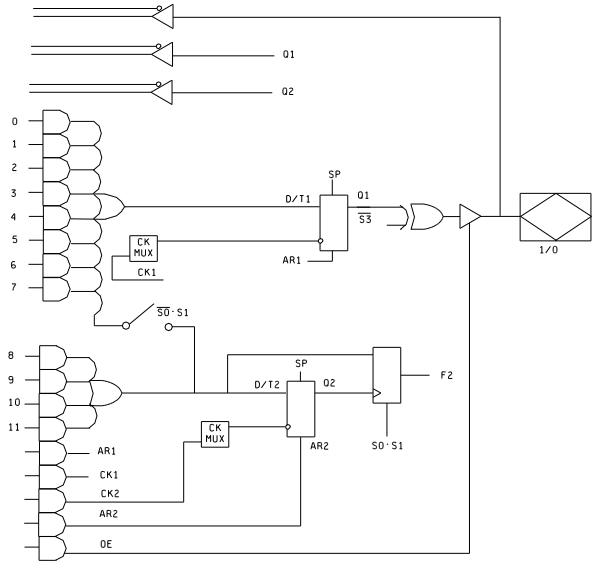
S3	Output configuration
0	Active low
1	Active high

S3	Output configuration
0	Active low
1	Active high

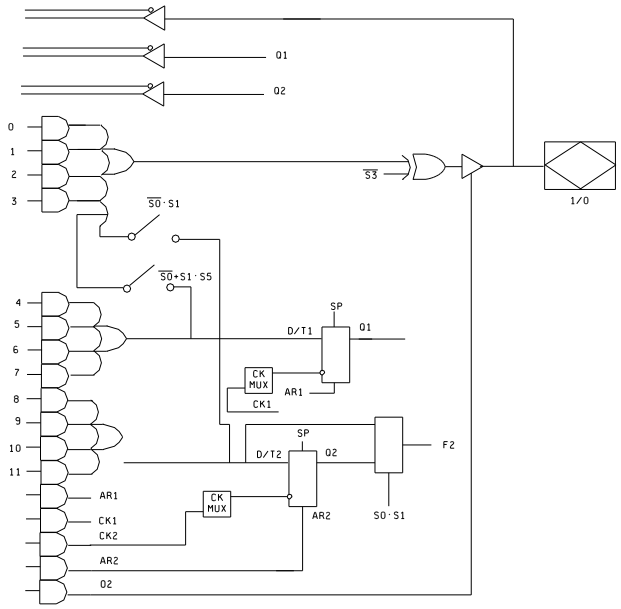
NOTE: These 4 terms are shared with D1.

FIGURE 4. Block diagram devices 01-03.

Output logic, registered



Output logic, combinational



NOTE: These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

S2 = 0 S1	S0	Terms in D/T1	D/T2	Output configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4*	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

* (See note)

S2 = 1 S5	S1	S0	Terms in D/T1	D/T2	Output configuration
X	0	0	4*	4	Combinatorial (8 terms); Q2 FB
X	0	1	4	4	Combinatorial (4 terms); Q2 FB
X	1	0	4*	4*	Combinatorial (12 terms); Q2 FB
1	1	1	4*	4	Combinatorial (8 terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 terms); D/T2 FB

* (See note)

S3	Output configuration
0	Active low
1	Active high

S4	Register 1 Type
0	D
1	T

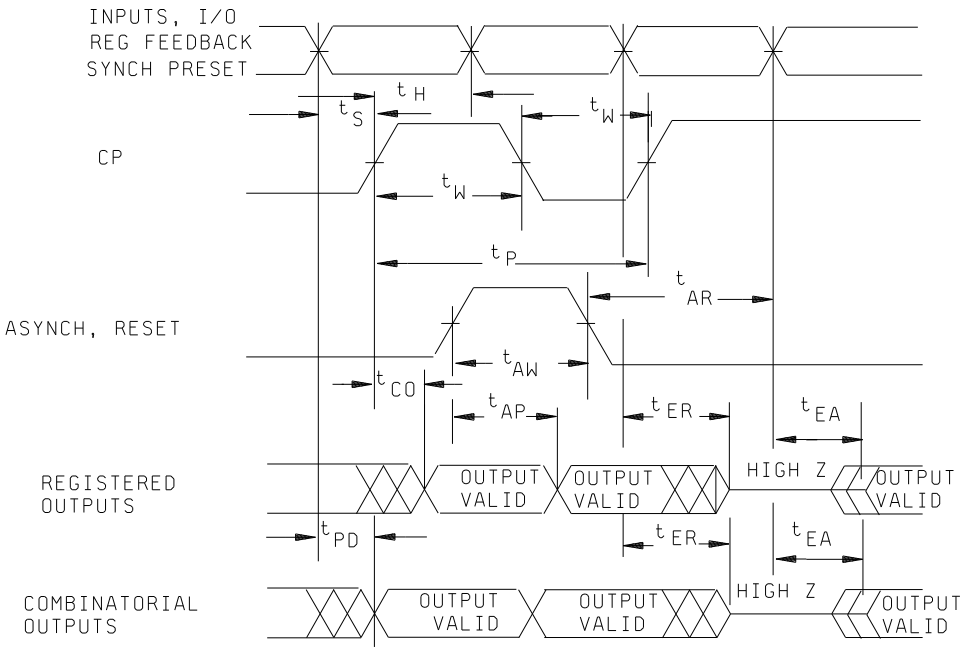
S5	Register 2 Type
0	D
1	T

S6	Q1 CLOCK
0	CK1
1	CK1 + PIN1

S7	Q2 CLOCK
0	CK2
1	CK2 + PIN1

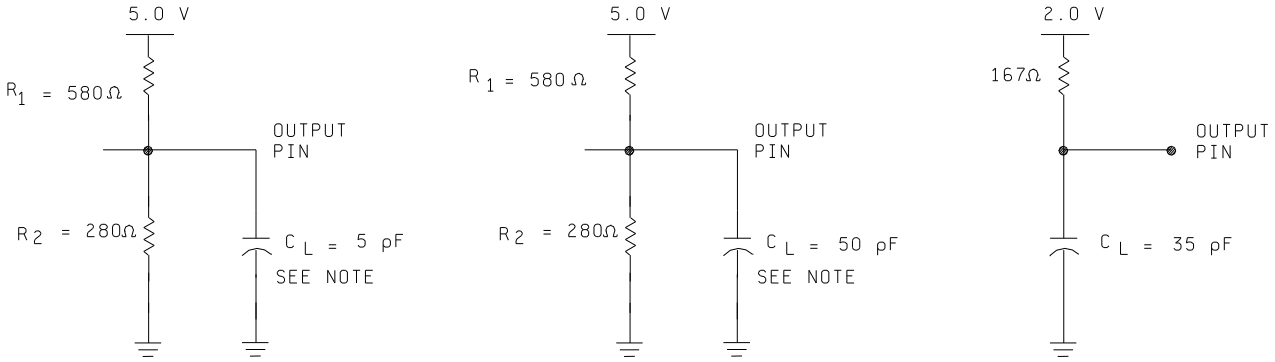
NOTE: These 4 terms are shared with D/T1.

FIGURE 4. Block diagram - Continued, devices 04-07.



NOTE: Timing measurement reference is 1.5 V. Unless otherwise specified, input ac driving levels are 0.0 V and 3.0 V.

FIGURE 5. Timing waveforms.



Circuit A or equivalent
All devices
(See note)

Circuit B or equivalent
Device types 01-03
(See note)

Circuit C or equivalent
Device types 04-07
(See note)

NOTE: Including jig and scope (minimum value).

FIGURE 6. Load circuits.

e. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups B, C, and D testing).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M . Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H; and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5° C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2,537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 ws/cm^2 (1 week at 12,000 uW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance
GND	Ground zero voltage potential
I_{CC}	Supply current
I_{LI}	Input load current
T_C	Case temperature
T_A	Ambient temperature
V_{CC}	Positive supply voltage
O/V	Latch-up over-voltage
O/I	Latch-up over-current

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
6	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
7	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
8	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
9	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{IH}	±1.0 µA of specified value in table I
I_{IL}	±1.0 µA of specified value in table I
I_{OZ}	±1.0 µA of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:

t X X X X

Signal name from which interval is defined

Transition direction for first signal

Signal name to which interval is defined

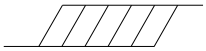
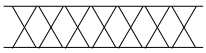
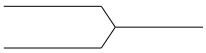
Transition direction for second signal

a. Signal definitions:
A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable

b. Transition definitions:
H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 95-05-19

Approved sources of supply for SMD 5962-91545 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9154501MQX	1FN41	ATV2500H-35DM/883
5962-9154501MXX	1FN41	ATV2500H-35LM/883
5962-9154501MYX	1FN41	ATV2500H-35KM/883
5962-9154502MQX	1FN41	ATV2500H-25DM/883
5962-9154502MXX	1FN41	ATV2500H-25LM/883
5962-9154502MYX	1FN41	ATV2500H-25KM/883
5962-9154503MQX	1FN41	ATV2500L-30DM/883
5962-9154503MXX	1FN41	ATV2500L-30LM/883
5962-9154503MYX	1FN41	ATV2500L-30KM/883
5962-9154504MXX	1FN41	ATV2500B-15LM/883
5962-9154504MYX	1FN41	ATV2500B-15KM/883
5962-9154505MXX	1FN41	ATV2500BL-20LM/883
5962-9154505MYX	1FN41	ATV2500BL-20KM/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9154506MXX	1FN41	ATV2500BQ-25LM/883
5962-9154506MYX	1FN41	ATV2500BQ-25KM/883
5962-9154507MXX	1FN41	ATV2500BQL-30LM/883
5962-9154507MYX	1FN41	ATV2500BQL-30KM/883

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Margin test method
1FN41	ATMEL Corporation 2125 O'Nel Drive San Jose, CA 95131	A

The information contained herein is dissemiated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.